DETAILED ACTION

Response to Arguments

Comments of the Examiner

Applicants arguments filed September 14, 2004 have been fully considered but they are not persuasive.

Applicant argues that Kaplan's patent is not relevant, since it does not show anywhere charge multiplication CCD stages between the CCD wells 14,16. In response to this argument that the references fail to show certain features of applicants invention, it is noted that the features upon which applicant relies (i.e., charge multiplication CCD stages between the CCD wells) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 958 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant also argues that in FIG. 1 of Kaplan it shows that (24) is an amplifier, not a charge multiplier and that the charge multiplication stages are incorporated between the wells of a serial register. However, the examiner is interpreting the amplifier in Kaplan to be the equivalent of a charge multiplier since both multiply a signal in order to change the output. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the charge multiplication stages are incorporated between the wells of a serial register) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181,26 USPO2d 1057 (Fed. Cir. 1993).

Reply to the Examiner's Comments (See Underlined)

In Kaplan's patent, and in all known charge detection amplifiers, the signal is first input as charge, then the signal becomes voltage or current and finally the output signal is still voltage or current.

In charge multipliers the signal is charged, it is multiplied as charge, and output is still charge. That is why it can stay in the CCD register. In all other charge amplifiers, charge signal is converted to another signal out side of CCD register. This is clearly shown in Kaplan's patent.

Please recognize this difference between charge multiplier and charge detection amplifier. This is well know and understood in the art.

The examiner is mistaken. Charge cannot be simply amplified, since there is a well known law of charge conservation in physics. Charge would have to be first detected, converted to a voltage or current, these then amplified by known transistor devices and then the amplified voltage or curent output would have to control injection of new charge from some charge reservoir back into the CCD register. This is nowhere shown or implied in the Kaplans

invention. Only the charge multiplication not charge amplification by the present invention is known in the art now.

Applicant also argues that the Kaplan invention shows registers (14) located in the image sensing area (10) coupled to photodiodes (12), and that in applicant's invention the registers are not located in the image sensing area and are not coupled to photodiodes. However, the examiner points out that the claim does not state that the registers are separate from the image sensor or that they are not coupled to photo diodes.

Reply to the Examiner's Comments (See Underlined)

This comment is strange, since the invention is not related to photodiodes, why should it mention this feature. While the Kaplan's invention is clearly related to photodiodes and the charge received from them is handled by adjacent registers. So this is why Kaplan's invention cannot be anticilpated for the charge multiplying registers without photodiodes.

Applicant also argues that in the Kaplan invention the charge is not transferred from one register to another, and moreover, it is not multiplied. However, the examiner disagrees, in Kaplan, the charge is transferred from one register to another (column 5, lines 1-8 the overflow charge is transferred from the first register 14 to the second register 16) and multiplied (column 4, lines 40-42).

Reply to the Examiner's comments (See Underlined)

The applicant did not find in this reference any mention of charge multiplication. The sentence in line 40-42 clearly states

that charge is clocked out into the amplifiers 24, 25. This clearly means out of the registers into the charge detection nodes of amplifiers where the signal charge is converted into a signal voltage and the voltage amplified as is well known in the art. The amplifier is not a charge multiplier and cannot and does not mean the same as is implied by the examiner.

Charge multiplication is done entire in charge domain of CCD registers, while in Kaplan's patent, amplification is done outside of the CCD register and not in charge domain.

Applicant argues that the charge amount is not increasing during the readout and transfer from one COD well (16) to another CCD well (16) and to the amplifier AMP (25). In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the charge amount is increases during the readout and transfer from one well to another well and to the amplifier) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that in Kaplan the anti-blooming overflow gate (31) is located on the other side (above) the photo diodes, not in any serial register. However, the examiner has not relied upon the overflow gate (31) in the rejection, the overflow gate that the examiner has relied upon is overflow barrier (22) as can be seen in figure 3 as well as column 5, line 4.

Reply to the Examiner' Comments (See underlined)

Kaplan's reference does not show charge overflow from the register (CCD wells 14) into the overflow drain 32. Kaplan's reference shows overflow to drain only from photodiodes 12. It is not obvious from Kaplan's reference that another overflow barrier and drain should be placed next to the CCD register with wells 16.

Applicant argues that in the present invention there are no photodiodes adjacent to registers, that charge is not supplied to registers in parallel (vertical) direction, and that charge is transferred in the horizontal direction and register has charge multiplication stages incorporated between register wells. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., no photodiodes adjacent to registers, that charge is not supplied to registers in parallel direction, and that charge is transferred in the horizontal direction and register has charge multiplication stages incorporated between register wells) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See/n *re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that in the present invention that as the amount of transported charge increases due to the multiplication process, OCD wells need to be made wider to accommodate larger amount of charge and that when the charge reaches the overflow area it overflows from one register to the other and further ~o an overflow drain while it is being transferred in the horizontal direction. As for the limitation that when the charge reaches the overflow area it overflows from one register to the other and further to an overflow drain while it is being transferred in the horizontal direction, Kaplan does teach this in column 5, lines 1-8. As for the limitation of the amount of transported charge increasing due to the multiplication process before overflow from one register to another and transfer to an overflow, this limitation is not claimed. As for the limitation of COD wells need to be made wider, Kaplan was not relied upon to teach this limitation.

Applicant also argues that in Kaplan there is no charge increase and the transfer of charge from one register to another is not expected during the horizontal charge transfer.

Applicant argues, with respect to claim 2, that Kaplan's invention charge is not transferred from one register to the other during the process of horizontal transfer to the detection node. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., charge is transferred from one register to the other during the process of horizontal transfer to the detection node) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that none of the references (Kaplan, Farrier, and Burt) explain that charge overflows from one register to the other due to one register being narrower and not being able to accommodate the transported charge. However, the examiner disagrees, Kaplan teaches that charge overflows from one register to the other due to

one register being narrower and not being able to accommodate the transported charge (column 5, lines 1-8).

Applicant argues, with respect to claim 3, that the present invention does not claim that the signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula. The examiner points out that this is the limitation as claimed in claim 3, and that if this reply is correct in the fact that the present invention does not make such a claim, then applicant should cancel claim 3.

Applicant argues that Kaplan does not include anywhere in its structure charge multipliers (24 and 26), and that it uses only charge detectors with amplifiers (24 and 25). The examiner points out that "charge multipliers (24 and 26y' was incorrectly reference before, and that it should read "charge multipliers (24 and 25)u, and that charge amplifiers (24 and 25) are considered to be the charge multipliers.

Applicant argues that in Kaplan, the charge cannot overflow from one register to another during the horizontal transport to detection node and amplifier one stage at a time. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which

applicant relies (i.e.,charge overflows from one register to another during the horizontal transport one stage at a time) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *inre Van* Geuns, 988 F.2d 1181,26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that there is no mention of charge multiplier in Butts column 4, line 55, and that there are no charge multipliers in Burt's FIG. 1: Sand 10. However, the examiner points out that although there is not mention of a charge multiplier in column 4, lines 55, it is mentioned in the lines following (column 4, lines 55-64) as cited in the previous rejection and has been pasted below:

> "To achieve multiplication of charge in each of the elements of the multiplication register 5, sufficiently high amplitude drive pulses are applied to control electrodes 10 to both transfer signal charge from one element to the next adjacent element in the direction shown by the arrow and also to increase the level of signal charge by an amount determined by the amplitude of the drive pulses.'

Claim Rejections - 35 USC 5102

Claims 1-3 and 9 have been rejected under 35 U.S.C. 102(b) as being anticipated by Kaplan (US Patent# 5,867,215).

Comments of the Examiner under the Rejection

In regard to claim 1, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture that incorporates charge multipliers (24), said image sensor including a first CCD register (14) adjacent to at least a second CCD register (16) and coupled to the said first register through a charge overflow barrier (22), where charge may overflow during transfer (column 5, lines 1-8).

In regard to claim 2, note Kaplan discloses the use of that the second adjacent CCD register collects overflow charge (column 4, lines 33-39; the overflow charge is sent to the second CCD register, 16) and

transports it to at least one detection node located in each register (column 4, lines 40-51; the transport of the signal from the CCD well to the amplifier is considered to be the equivalent of the detection node), and each charge detection node having charge conversion sensitivity that may be different for each node (column 5, lines 1-6; although not explicitly stated, it is inherent that the sensitivity changes with respect to the charge handling capabilities, and the CCD registers, 14 and 16, are of different charge handling capabilities).

In regard to claim 3, note Kaplan discloses that the signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula (column 5, lines 45-61).

In regard to claim 9, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture, said readout architecture incorporating charge multipliers (24 and 25), OCD registers (14 and 16), and a charge overflow device in at least one of its registers (22).

Reply to the Examiner's comments (see Underlined)

Please do not misstate the Kaplan's sentences. Nowhere in the Kaplan's invention Kaplan mentions charge multipliers, only amplifiers. As has been already mention these cannot be made equal in meaning as is well known in the art.

Claims Amendments

Claims 1, 4 and 8-9 have been amended to include the allowable subject matter.

Claim Rejections - *35 USC 5103*

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (US Patent #6,444,968) in view of Farrier et al. (US Patent #6,392,260).

Comments of the Examiner under the Rejection

In regard to claim 4, note Burt discloses the use of a solid-state image sensor (2) having a readout architecture that incorporates charge multipliers (column 4, lines 55-64; and figure 1: 5 and 10), said image sensor including: a CCD register that incorporates at least one charge-multiplication device element in at least one stage (column 4, lines 55-64; and figure 1:5 and 10). Therefore, it can be seen that the Burt device lacks the use of said at least one stage having a progressively wider width. Farrier discloses the use of a CCD register having a progressively wider width (column 7, line 66— column 8, line 28; and figure 3: 110). Farrier teaches that the use of a progressively wider width is preferred in order to carry all the charge transferred without blooming (column 8, lines 25-28). Therefore, it would have been obvious to one of ordinary skill in the art to modify the Burt device to include the use of a progressively wider width as suggested by Farrier.

Allowable Subject Matter

Comments of the Examiner

Claims 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As for claims 5, the prior art does not teach or fairly suggest the use of a solid-state image sensor having a readout architecture having a CCD register having a progressively wider width, wherein the width of the register and the number of charge multiplication elements varies according to a predetermined formula.

Reply to the Examiner's Comments

Claims 1, 4 and 8-9 have been amended to include the allowable subject matter.

Summary

Since the claims have been amended to include the allowable limitations, it is respectfully requested that the claims be allowed and the application passed to issue.

Respectfully submitted,

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